FPGA-Based Control Board
User Manual

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Engineering

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The First course in Power Electronics covers the operation of dc-dc and dc-ac converters such as buck converter, boost converter and buck-boost converters (along with their transformer isolated counterparts, forward and flyback converters) and single phase and three phase inverters. These converters are controlled using analog circuitry present on the Power-Pole board in the Power Electronics Lab and using dSPACE on the Inverter board. An FPGA control board can be used for controlling these converters. This board is capable of closed-loop operation when interfaced with the Power-Pole board and open-loop operation with the Inverter board.

Safety warning: This Control board is intended for use in the Power Electronics and Electric Drives labs. While performing any experiment, the safety precautions of the lab should be followed. Refer to the respective lab manuals for these important safety measures.

Contents

1 Getting Started **2**
- 1.1 Board Layout . . . 2
- 1.2 Downloading Configuration File . . . 2
- 1.3 Preparing the Power-Pole Interface Cable . . . 5
- 1.4 User Interface . . . 6

2 PWM for Open-Loop DC-DC Converters (Experiment 1) **7**
- 2.1 Objective . . . 7
- 2.2 Performing the Experiments . . . 7

3 Closed-Loop DC-DC Buck Converter (Experiment 2) **8**
- 3.1 Objective . . . 8
- 3.2 Determine the Transfer Function . . . 8
- 3.3 Designing the Controller . . . 8
- 3.4 Preparing the Setup . . . 11
- 3.5 Measurement and Waveforms . . . 11
  - 3.5.1 Varying the Load . . . 11
  - 3.5.2 Varying the Reference . . . 11

4 Three-Phase Inverter (Experiment 3) **12**
- 4.1 Objective . . . 12
- 4.2 Preparing the Setup . . . 12
  - 4.2.1 Varying the Frequency . . . 12

1 Getting Started

1.1 Board Layout

At the core of the control board, is a Xilinx® Spartan®-3E FPGA which is configurable by an on-board PROM. The configuration file (.bit) can be downloaded into the PROM using a USB/JTAG interface module. Also present on the board is a 12-bit multiplexed dual-channel ADC to perform closed-loop control experiments. The layout of the various components are shown in Fig. 1.

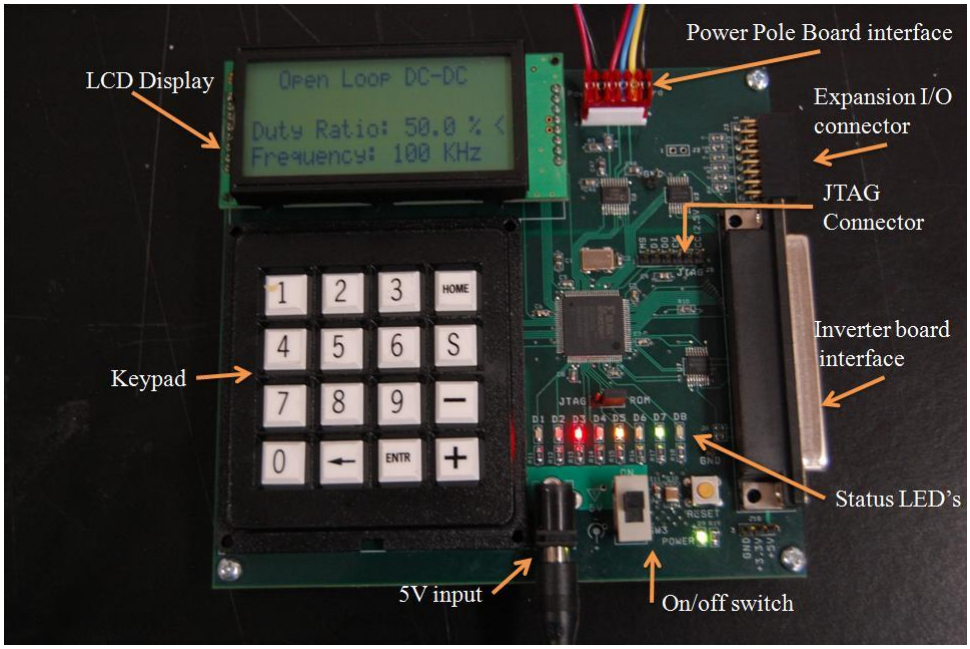

Figure 1: FPGA Control Board

1.2 Downloading Configuration File

Before using the board, make sure the board is running the latest version of the configuration file. This latest version can be found at the University of Minnesota, Electric Energy Systems group website `http://www.ece.umn.edu/groups/power/mat_lab.html`.

1. Download the latest .bit file from the Laboratories section of the webpage.
2. If you do not already have Digilent Adept installed, install the latest version from the Digilent Inc. website `http://www.digilentinc.com`
3. Connect the Digilent JTAG-USB Full Speed Module to an available USB port and follow on-screen instructions to install the appropriate device drivers.

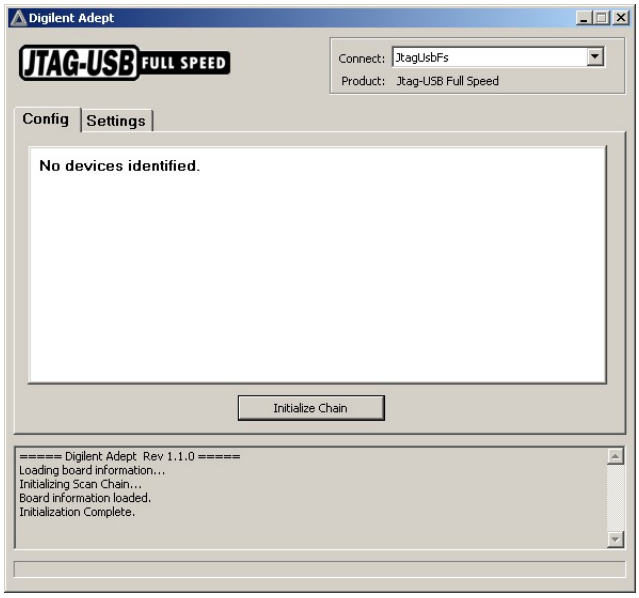

Figure 2: Digilent Adept main window

4. With the JTAG-USB module still connected, open Digilent Adept. The main window opens as shown in Fig. 2.

5. Connect the JTAG-USB module to the JTAG connector (J5) of the FPGA control board. Make sure the module is properly aligned with the pin names on the board matching those on the module.

6. Plug in the 5V dc power supply to the FPGA control board and turn on the power switch.

7. Click 'Initialize Chain' in the Digilent Adept window. The software should recognize the FPGA (XC3S250E) and the PROM (XCF02S) as shown in Fig. 3.

8. Click the 'Browse' button next the PROM and select the .bit file.

9. Download the .bit file into the PROM by clicking the 'Program' button. When successfully completed, the status message shown in Fig. 4 should appear.

10. Turn off the FPGA control board and disconnect the JTAG-USB module.

11. Make sure the configuration jumper (J7) is set to ROM-mode and turn on the board. The FPGA is now configured with the new .bit file.

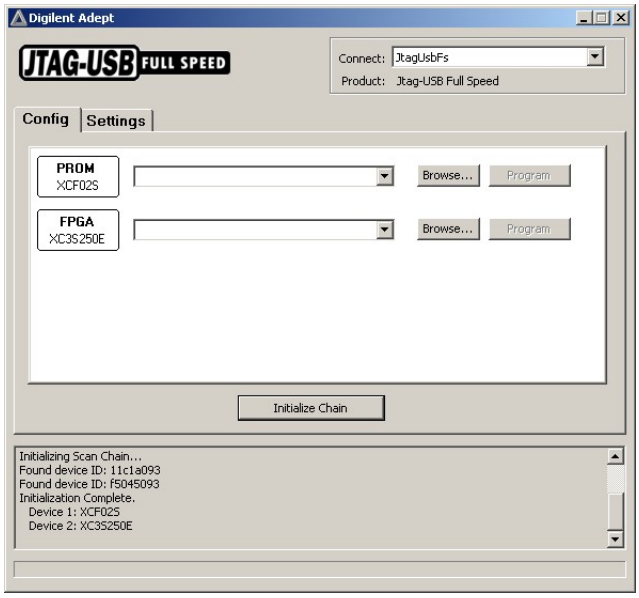

Figure 3: Digilent Adept: JTAG Chain Initialized

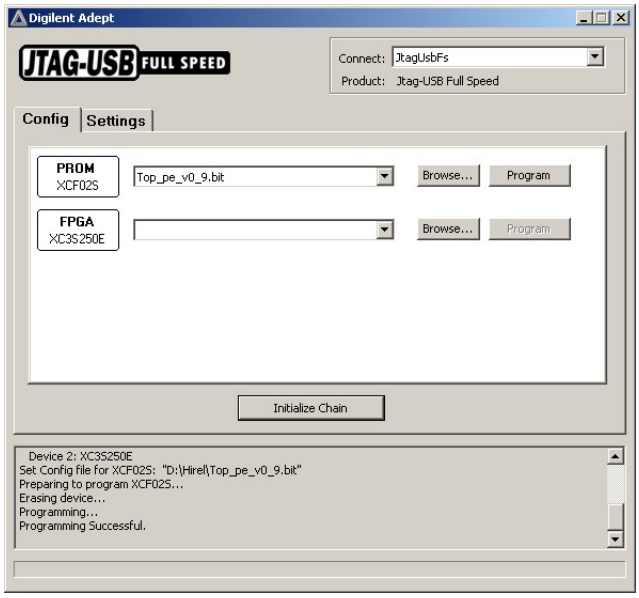

Figure 4: Digilent Adept: Program downloaded successfully

1.3 Preparing the Power-Pole Interface Cable

The supplied Power-Pole board interface cable has to be soldered to a blank daughter board which plugs into J60 of the Power-Pole board. Note that this daughter board is the proto-board that is used in the voltage mode control and current mode control experiments of the Power Electronics lab. Solder the wires according to Table 1. The soldered cable is shown in Fig. 5

Table 1: Power-Pole Board Interface

FPGA Control Board (J1)		Power Pole Board	
Pin	Color	Pin	Name
1	Red	J68(+)	PWM
2	Black	J68(-)	GND
3	Red	J60(Pin 9)	V2/5
4	Blue	J60(Pin 7)	CURRENT1
5	Yellow	J60(Pin 11)	CURRENT2
6	Black	J60(Pin 19)	GND

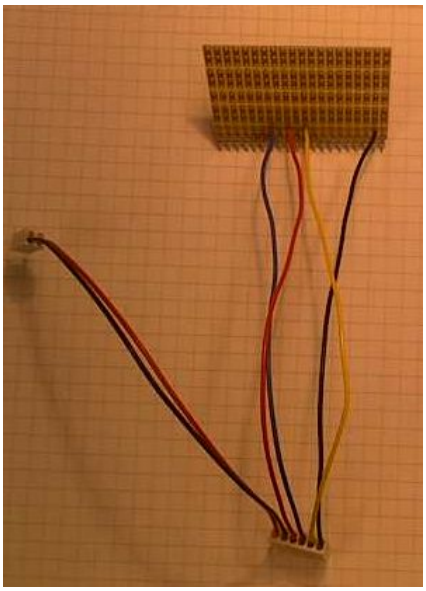

Figure 5: Power-pole board interface cable

1.4 User Interface

The main user interface is the LCD display for output and the keypad for input. Using this interface, the user can navigate between the different modes of operation of the control board and change experiment parameters. The keypad functions are give in table 2.

Table 2: Keypad Functions

Key	Function
1-9	Enter numeric data
0	Enter numeric data/ Reset
HOME	Terminate current operation and return to startup screen
ENTR	Confirm selection
←	Delete most recently entered character
S	Toggle between parameters that can be changed
+	Increase the selected parameter
-	Decrease the selected parameter/ Negative sign

2 PWM for Open-Loop DC-DC Converters (Experiment 1)

2.1 Objective

The FPGA Control Board is used to generate variable frequency PWM pulses. These pulses can be used for open loop control of the following Power Electronics Laboratory experiments.

1. Buck Converter
2. Switching Characteristic of MOSFET and Diode
3. Boost Converter
4. Buck-Boost Converter
5. Flyback Converter
6. Forward Converter

2.2 Performing the Experiments

Connect the FPGA Control board to the Power-Pole board using the Power-Pole board interface cable (Fig. 5). After powering on the FPGA Control board, input 1 at at the startup screen and press ENTR. This executes the open-loop PWM generation module. In the above mentioned set of experiments, either the frequency or the duty ratio is to be varied. The key 'S' on the keypad is used to make this selection. The frequency of the PWM pulse can be varied from 50 kHz to 200 kHz in steps of 10 kHz and the duty ratio of the PWM pulses can be varied from 0 to 0.9 in steps of 0.025 using the ' + ' or ' - ' keys on the keypad on the FPGA board. Follow the instructions for the respective experiments as detailed in the Power Electronics Lab Manual. Make sure that the switch 2 of S30 on the Power-Pole board is set to PWM EXT.

3 Closed-Loop DC-DC Buck Converter (Experiment 2)

3.1 Objective

The objective is to design a digital voltage-mode controller for a buck converter.

3.2 Determine the Transfer Function

The small-signal transfer function $G_{ps}(s)$ must first be obtained either by simulation or by experimentation. $G_{ps}(s) = \tilde{v}_o(s)/\tilde{d}(s)$

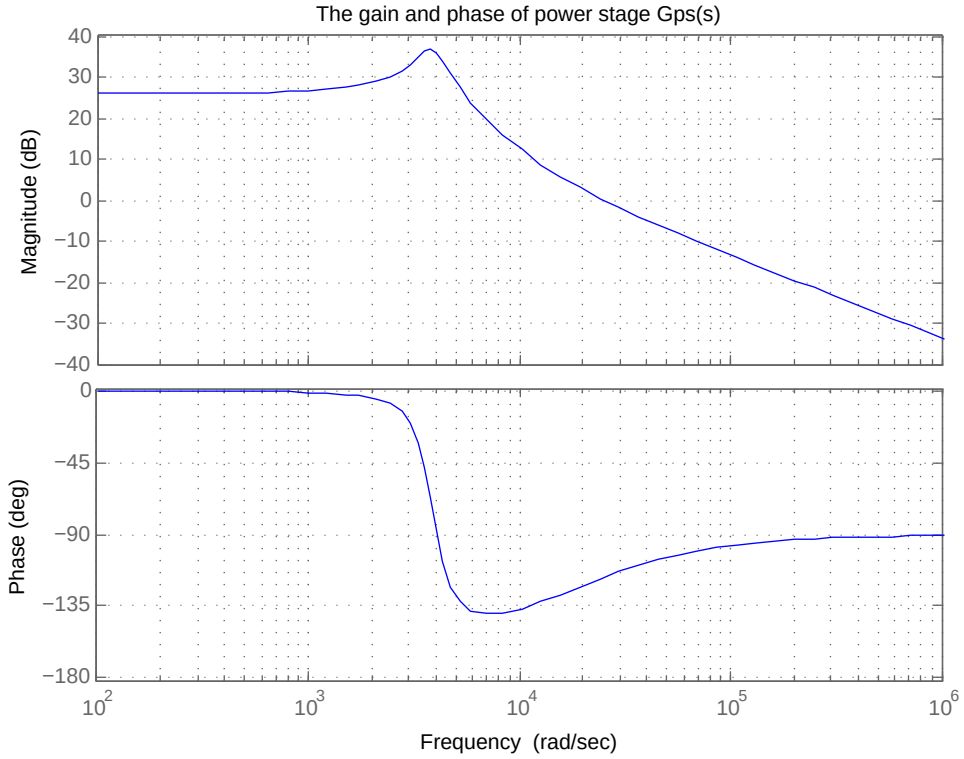

Figure 6: The Gain and Phase of Power Stage.

- Simulate the circuit in PSpice (buck_conv_avg.sch) and obtain the bode plot for $\tilde{v}_o(s)/\tilde{d}(s)$ as shown in Figure 6.
- Select a crossover frequency f_c. **Note:** the crossover frequency is the frequency at which the gain equals to 0dB. The value of f_c is generally chosen just beyond the L-C resonance frequency.
- Measure the gain and phase of the transfer function $\tilde{v}_o(s)/\tilde{d}(s)$ at f_c.

3.3 Designing the Controller

With gain and phase of the buck converter at the crossover frequency, the controller can be designed to obtain the desired regulation in output voltage.

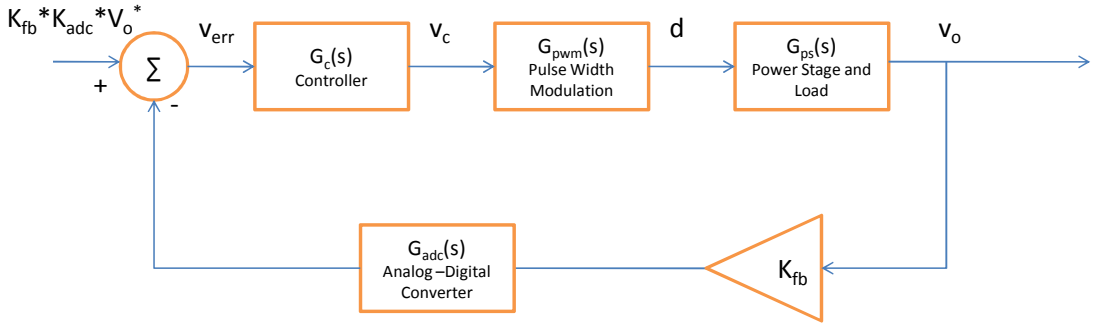

Figure 7: Block diagram of Buck converter with Voltage Mode Control

- The controller $G_c(s)$, given by equation (1) can be designed using the steps given in the text book, First Course on Power Electronics by Ned Mohan (Section 4-4).

$$G_c(s) = \frac{kc\left(1+\frac{s}{\omega_z}\right)^2}{s\left(1+\frac{s}{\omega_p}\right)^2} \tag{1}$$

$$\begin{aligned} |G_{fb}(s)| &= K_{fb} = 0.2 \times 0.6 = 0.12 \\ |G_{adc}(s)| &= \frac{1}{0.0012207} \cdots \text{as 5V} = 4096 \text{ bits.} \\ |G_{pwm}(s)| &= \frac{1}{2000} \cdots \text{sawtooth waveform counts from 0 to 2000.} \end{aligned} \tag{2}$$

  Where, $|G_{fb}(s)|$ is the gain of the analog feedback amplifier on the board, $|G_{adc}(s)|$ is the gain of the ADC, $|G_{pwm}(s)|$ is the gain of the sawtooth comparator.

- At the crossover frequency f_c, the open loop gain, $|G_L(s)|$ is 1.

$$|G_L(s)|_{f_c} = |G_c(s)|_{f_c} \times |G_{fb}(s)|_{f_c} \times |G_{adc}(s)|_{f_c} \times |G_{pwm}(s)|_{f_c} \times |G_{ps}(s)|_{f_c} = 1 \tag{3}$$

- The discrete equivalent, $G_c(z)$ of $G_c(s)$ can be obtained using the Tustins approximation. This transformation can be obtained by replacing 's' in (1) by (4)
  The sampling frequency, f_s is set at 10kHz.

$$s = \frac{2}{T} \cdot \frac{(z-1)}{(z+1)} \tag{4}$$
$$\text{Where,} T = \frac{1}{f_s}$$

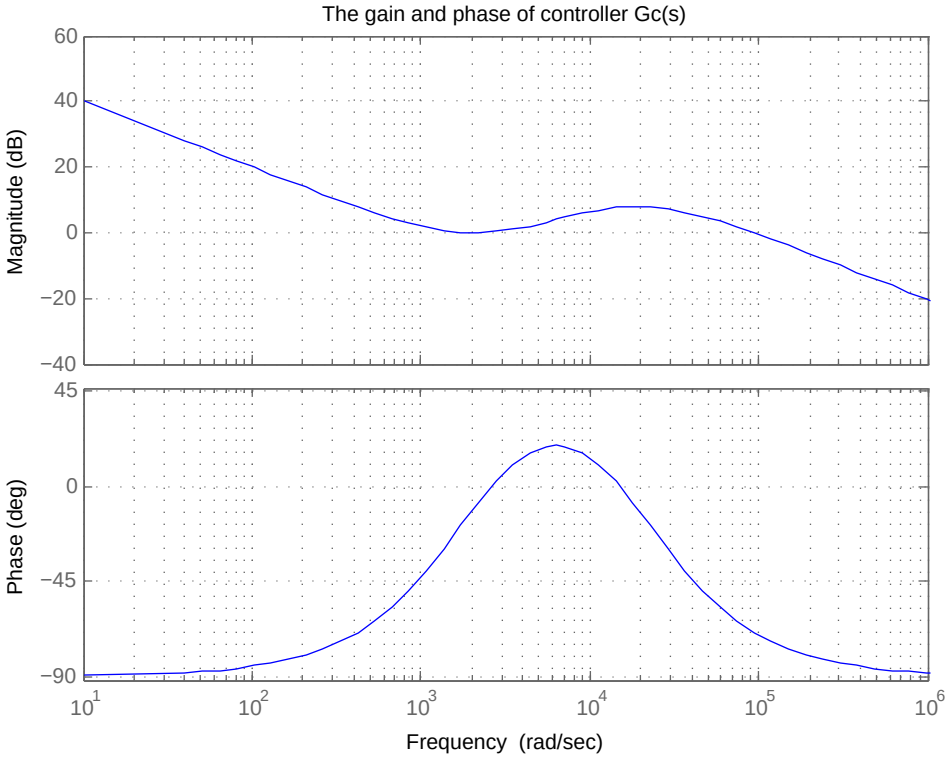

Figure 8: The Gain and Phase of the Controller

$G_c(z)$ is given by (5)

$$G_c(z) = \frac{a_1 z^3 + a_2 z^2 + a_3 z + a_4}{b_1 z^3 + b_2 z^2 + b_3 z + b_4} \tag{5}$$

- The values of a_1,a_2,a_3,a_4,b_1,b_2,b_3 and b_4 can be calculated as using the equations below

$$\begin{aligned}
K &= kc\frac{(\omega_p/\omega_z)^2}{2f_s} \\
a_1 &= K(\omega_z^2 + (2f_s)^2 + 4f_s\omega_z) \\
a_2 &= K(3\omega_z^2 - 4f_s^2 + 4f_s\omega_z) \\
a_3 &= K(3\omega_z^2 - 4f_s^2 - 4f_s\omega_z) \\
a_4 &= K(\omega_z^2 + 4f_s^2 - 4f_s\omega_z) \\
b_1 &= \omega_p^2 + (2f_s)^2 + 4f_s\omega_p \\
b_2 &= \omega_p^2 - 12f_s^2 - 4f_s\omega_p \\
b_3 &= -\omega_p^2 + 12f_s^2 - 4f_s\omega_p \\
b_4 &= -(\omega_p^2 + (2f_s)^2 - 4f_s\omega_p)
\end{aligned} \tag{6}$$

$$\begin{bmatrix} A1 \\ A2 \\ A3 \\ A4 \\ B1 \\ B2 \\ B3 \\ B4 \end{bmatrix} = (2^7) \cdot \frac{1}{b_1} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ -b_1 \\ -b_2 \\ -b_3 \\ -b_4 \end{bmatrix} \tag{7}$$

- Round off A1 , A2 , A3 , A4 ,B1, B2 ,B3 and B4 to the nearest integer value.

3.4 Preparing the Setup

- Refer to the Voltage-Mode Control experiment of the Power Electronics Lab Manual. Make sure that the switch 2 of S30 on the Power pole board is set to PWM EXT.
- Connect the FPGA Control board and the Power-pole board using the power pole board interface cable(Fig. 5).
- After powering on the FPGA Control board, input 2 at at the startup screen and press ENTR. This executes the closed-loop PWM generation module.
- Using the keypad, enter the coefficients A1, A2, A3, A4, B1, B2, B3 and B4 in the FPGA Control Board.
- Set RL=20 ohms.
- Turn on the switched load (Switch 3 of S30).
- Turn ON the ±12 V signal supply and check for green LED.
- Have the circuit checked by the lab instructor.
- Set Vd to 24 V.

3.5 Measurement and Waveforms

3.5.1 Varying the Load

- Set the reference voltage at 5 V.
- Observe the Output Voltage V2+.
- Measure the value of peak overshoot.
- Measure the rise time.

3.5.2 Varying the Reference

- Vary the reference Voltage from 5 V to 10 V using the ‘ + ’ or ‘ - ’ keys on the keypad on the FPGA control board and observe the output voltage.

4 Three-Phase Inverter (Experiment 3)

4.1 Objective

The FPGA Control board generates PWM pulses for a three phase inverter. A variable frequency V/f control is implemented. This experiment is performed by connecting the FPGA Control board to the Inverter board.

4.2 Preparing the Setup

- Power on the Inverter board by following instructions from the Electric Drives Lab manual and connect a three phase induction motor to the output of Inverter 1.
- Connect the FPGA Control board and the Inverter board using a 37 pin DSUB cable.
- After powering on the FPGA Control board, input 3 at the startup screen and press ENTR. This executes the Three phase V/f PWM generation module.

4.2.1 Varying the Frequency

The speed of the motor can be varied from 0 Hz to 200 Hz in steps of 5 Hz using the‘ + ’ or ‘ - ’ keys on the keypad on the FPGA board.